- On page 4, please delete the first full paragraph and replace it with the following paragraph:

B3 Figures 3A and 3B show a top view and a cross-sectional view respectively of the wafer of Figures 2A and 2B having a structural layer added thereon.

- On page 4, please delete the second paragraph and replace it with the following paragraph:

B4 Figures 4A and 4B show a top view and a cross-sectional view respectively of the wafer of Figures 3A and 3B having a second sacrificial layer deposited thereon.

- On page 4, please delete the third paragraph and replace it with the following paragraph:

B5 Figures 5A and 5B show a top view and a cross-sectional view respectively of the wafer of Figures 4A and 4B having a seal layer applied thereon.

- On page 4, please delete the fourth paragraph and replace it with the following paragraph:

B6 Figures 6A and 6B show a top view and a cross-sectional view respectively of the wafer of Figures 5A and 5B having etch holes drawn therein.

- On page 4, please delete the fifth paragraph and replace it with the following paragraph:

B7 Figures 7A, 7B and 7C show a top view, a cross-sectional view along line 7B and a cross-sectional view along line 7C respectively of the wafer having the sacrificial layers removed by an enchant.

- On page 4, please delete the sixth paragraph and replace it with the following paragraph:

B8 Figures 8A and 8B show a top view and a cross-sectional view respectively of the wafer having a second seal layer applied thereon, thereby sealing the etch holes.

- On page 4, please delete the seventh paragraph and replace it with the following paragraph:

B9 Figures 9A and 9B show a top view and a cross-sectional view respectively of the second seal layer having been removed from the contact pad on the base wafer.

- On page 4, delet the ninth paragraph and replace it with the following paragraph:

B 10

Figures 1-9 illustrate the sequence of steps comprising the fabrication of the proposed encapsulated integrated microstructure CMOS process. We start by obtaining or fabricating a silicon CMOS wafer 2 coated with a layer of silicon nitride 4 and having metal pads interfacing to the original CMOS integrated circuit 6, 8 and 10 present as shown. Openings appear in the silicon nitride layer 4 to allow access to metal pads 6 and 8. In the preferred embodiment, the metal pads would be aluminum, but may alternatively be copper or any other conductive material.

- On page 5, please delete the first full paragraph and replace it with the following paragraph:

B 11

To begin the fabrication process, a sacrificial layer 12 is deposited on top of the passivation layer of the standard CMOS wafer 2, which in this case is silicon nitride layer 4. The MEMS device fabrication steps are all performed at low temperature on top of the complete CMOS wafer 2, leaving the circuitry therein undisturbed. Cuts in the passivation layer 4 are left during the CMOS IC design and sacrificial layer 12 is removed over these cuts if access to the metal contacts is desired. The exposed metal contacts 6 and 8 are then used to make connections between the MEMS microstructure and the CMOS circuitry in silicon CMOS wafer 2 below. This is illustrated in Figure 2A.

- On page 5, please delete the third full paragraph and replace it with the following paragraph:

B 12

The deposition of the MEMS layer is shown in Fig. 3A and in cross section in Fig 3B. MEMS microstructure 14 is deposited by methods known by those with ordinary skill in the art and the undesirable portions are etched away, thereby leaving the desired shape of the microstructure behind. The top view of Figure 3B clearly shows the shape of the microstructure as being a paddle having a long thin beam attached to an anchor point, which in this case is metal contact 8.

- On page 5, please delete the fourth full paragraph and replace it with the following paragraph:

B13 Next, as shown in Fig. 4A, and in cross section in Fig. 4B, a second sacrificial layer 16 is deposited over the microstructure. It can be seen from the top view that portions of the top sacrificial layer 16 will come into contact with portions of the b ttom sacrificial layer 12, in particular, those areas near the edges of the paddle-shaped main body of the microstructure and those areas on either side of the thin connecting beam portion of the microstructure.

On page 6, delete the first full paragraph and replace it with the following paragraph:

B14 The preferred material for sacrificial layers 12 and 14 is photoresist. Photoresist is chosen for this reason because it can be etched with an oxygen plasma gas, which is not destructive of aluminum microstructure 14, silicon nitride passivation layer 4 or seal layer 18. Figures 4A and 4B show the deposition of second sacrificial layer 16.

On page 6, delete the fourth full paragraph and replace it with the following paragraph:

B15 Figures 5A and 5B show the deposition of seal layer 18. This layer may be composed of an insulator or a conductor, depending on the desired electrical operation of the microstructure. Additionally, the seal layer must have a low enough residual stress and must be thick enough that the membrane created by the seal layer 18 will not buckle after the sacrificial layers 12 and 16 have been removed. In the preferred embodiment, seal layer 18 is the same metal as was chosen for the microstructure layer 14, but in alternate embodiments may be made of any material resistant to the etchant chosen. In the event an insulating material is chosen for seal layer 18, it may be patterned and removed to give access to the non-MEMS parts of the integrated circuit, such as bond pads 6 and 8. If seal layer 18 is a conductor, it may be contacting one or both of bond pads 6 or 8.

On pages 6 and 7, delete the paragraph beginning on page 6 and ending on page 7 with the following paragraph:

B16 Next, one or more etchant access holes 20, shown in Fig. 6A and 6B are etched into seal layer 18 such that communication can be established with sacrificial layers 12 and 16. This etch is done by any means well known to anyone of ordinary skill in the art. Preferably etch holes 20 will be as far away as p ssible from the actual MEMS microstructure. Next, as shown in Figs. 7A, 7B and 7C, the etchant is introduced into holes 20 and sacrificial layers 12 and 16 are etched

away, leaving void 22. Figure 7B shows a cross-sectional view of th device through the center, while Figure 7C sh ws a cross-sectional view through one of the etchant access holes. A dry plasma etchant is used to avoid problems created by the surface tension of a wet etchant. In the preferred embodiment, the etchant is oxygen plasma. Oxygen plasma was chosen because it is highly selective with respect to the etching sacrificial layers 12 and 14, which may be photoresist or other organic polymers, while having an extremely low etching rate for a wide variety of metals and insulators.

B16 Cancel

- On page 7, please delete the second full paragraph and replace with the following paragraph:

The final step, shown in Fig. 8A, is the application of a second seal layer 26 to seal etch holes 20. In the preferred embodiment, seal layer 26 is the same metal as seal layer 18 and MEMS microstructure 14. As shown in Fig. 9, if the second seal layer is not a conductor then it may be etched away using well known methods from the area over contact pad 6, or it may be left in electrical contact with compact pad 6. Final seal layer 26 may be etched away from contact pad 6, or, if seal layer 26 is composed of a conductor, may be left in place.

B17

In the Claims:

- Please re-write claim 1 as follows:

Sub C' B18

1. A method of fabricating a microstructure in a sealed cavity comprising the steps of :

providing a substrate;

forming a microstructure composed of a structural material on said substrate in a sealed cavity, said microstructure being secured to said substrate at one or more points by a sacrificial material;

forming one or more holes in said sealed cavity;

introducing a non-liquid etchant into said sealed cavity through said one or more holes using a barrel etcher, said structural material and said sacrificial material having a high etch rate differential with respect to said etchant, such that said sacrificial material is removed; and

sealing said one or more holes in said sealed cavity.